TECHADYANT LABS

INSIGHTS | STRATEGY | IMPACT

BUILDING INDIA'S SEMICONDUCTOR ECOSYSTEM FOR THE WORLD

SEMICON 2.0 OPPORTUNITY MAP

Capturing the Next ₹10,000 Crore in India's Semiconductor Ecosystem (2025–2035)

A STRATEGIC ROADMAP TO CAPTURE 65% OF THE SEMICONDUCTOR VALUE CHAIN BEYOND FABS & OSAT

8 STREAMS
Materials | Chemicals | Equipment | Precision | Packaging | Testing | Automation | Industrial Software

₹45,500 CRORE
Serviceable Obtainable Market by 2035

0.48x CAPITAL EFFICIENCY
₹2.08 Value Creation per ₹1 Capital Deployed

3 SCENARIOS
Base | Accelerated | Constrained Outcomes by 2035

ACTIONABLE INTELLIGENCE
for Government, Investors, Corporates, Startups & Academia

₹52,500 – ₹92,000 CRORE
VALUE CREATION POTENTIAL BY 2035

NATIONAL PRIORITY
Strengthening Strategic Autonomy

ECONOMIC MULTIPLIER
High Value Jobs, Exports & GDP Impact

ECOSYSTEM DEVELOPMENT
From Manufacturing to Global Leadership

INNOVATION & TALENT
Building IP, R&D and Deep Tech Capability

GLOBAL COMPETITIVENESS
Positioning India as the Third Pole of Semiconductors

TECHADYANT LABS

STRATEGIC INTELLIGENCE

Semicon 2.0

Opportunity Map

Where India's Next Rs 45,500 Crore Semiconductor

Opportunities Will Emerge

EDITION	COVERAGE	AUDIENCE
Strategic Intelligence Report	8 Streams, 10-Year Horizon	CXOs, Investors, Policymakers

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About Techadyant Labs

Techadyant Labs is a strategic intelligence firm that produces premium research publications for CXOs, government officials, investors, and policymakers. Our work spans technology, industrial policy, geopolitics, and capital markets, with a focus on emerging opportunities in India and Asia.

Techadyant Labs is an independent, India-first strategic-intelligence practice. We map the industrial systems beneath India's technology ambitions - semiconductors, AI infrastructure, critical minerals, defence and enterprise sovereignty - and trace where value, dependency and opportunity actually sit. We are not a consultancy retained by the companies we cover; our only obligation is to the reader trying to make a decision.

Our mission is to produce strategic intelligence - not descriptive reports. Every chapter answers: What does this mean? So what? What should the reader do? What opportunities exist? What risks emerge? What changes over the next decade? Our publications are designed to drive decision-making, not merely to inform.

Every chapter is built to answer four questions: what is happening, why it matters, what it means for the reader, and what to do about it. We lead with the conclusion and support it with evidence, rather than burying the finding at the end.

For more information about Techadyant Labs publications, custom research, or strategic advisory services, visit www.labs.techadyant.com or contact info@labs.techadyant.com.

Editorial Note

The Semicon 2.0 Opportunity Map synthesises Techadyant Labs' research across government datasets, industry reports, policy papers, company filings, patent and procurement records, trade data and market intelligence, mapped onto the Labs' eight-stream framework for the semiconductor value chain.

The Executive Summary is structured as Situation, Complication and Resolution, and each chapter follows a consistent arc of situation, complication, analysis, evidence, strategic insight, implications, recommendations and outlook. Every chapter opens with an Executive Takeaway that states the key message in two to three sentences.

All market-sizing in this report is Techadyant Labs' own modelling, built from stated assumptions and presented as three scenarios - Base, Accelerated and Constrained. Figures are labelled by confidence: verified where confirmed by an official or industry primary source, estimated where triangulated from partial data, and modelled where derived from assumptions. The sizing should be read as directional estimates of opportunity, not as forecasts.

The report is designed to be read selectively or in full. The Executive Summary (10-15 pages) functions as a standalone briefing for CEOs and senior decision-makers. Individual chapters can be read in any order, with cross-references provided where relevant. Appendices provide additional strategic value through company databases, funding databases, policy trackers, and reference materials.

This report is published in four deliverables: (1) the Full Report (this document), (2) the Executive Edition (15-page standalone lead magnet), (3) the Excel Workbook (10 sheets of master data, company database, startup database, financial models, forecast assumptions, technology mapping, policy tracker, funding database, charts source data, and reading list), and (4) Figures Package (SVG and PNG exports of all exhibits).

How to Read this Report

This report is designed for selective or full reading. Different readers will find different sections most relevant to their roles and decision contexts. The following guidance helps readers navigate the report effectively based on their needs.

For CEOs and Senior Executives (15-minute read):
Read the Executive Summary (pages 12-25). This standalone briefing covers the major findings, strategic implications, investment thesis, and recommendations. Skip to Chapter 15 for the ten strategic imperatives if you need the actions first.

For Investors and PE/VC Professionals (45-minute read):
Read the Executive Summary, Chapter 2 (Opportunity Architecture), Chapter 12 (Investment Thesis), and Chapter 13 (Risk Outlook). The Excel Workbook provides supporting financial models and forecast assumptions. The investment matrix in Chapter 12 (Figure 10) provides the quick-screening framework.

For Government Officials and Policymakers (60-minute read):
Read the Executive Summary, Chapter 1 (Strategic Context), Chapter 11 (Cross-Cutting Enablers), and Chapter 15 (Strategic Recommendations). The policy tracker in Appendix C and the state-wise comparison in Appendix D provide additional context. Chapter 14 (10-Year Roadmap) provides the implementation framework.

For Corporate Strategy Teams (90-minute read):
Read the Executive Summary and the chapters specific to your stream(s) of interest (Chapters 3-10). Each chapter follows the same structure: Situation, Complication, Analysis, Evidence, Strategic Insight, Implications, Recommendations, Future Outlook. The company database in Appendix A provides competitive intelligence.

For Startup Founders and Entrepreneurs (45-minute read):
Read the Executive Summary, Chapter 10 (Industrial Software), Chapter 12 (Investment Thesis), and Chapter 15 (Strategic Recommendations). The startup database in Appendix B and the technology mapping in the Excel Workbook provide competitive landscape context.

For Academia and Research Community (90-minute read):
Read the full report, with particular attention to Chapter 11 (Cross-Cutting Enablers, including talent pipeline analysis) and the Methodology and Research Notes sections. The References section provides a curated reading list for further research.

Acknowledgements

This report is a synthesis of the public record of India's semiconductor build-out, mapped onto Techadyant Labs' eight-stream framework. All opinions, analyses and conclusions are those of Techadyant Labs alone.

It draws on the public disclosures of the companies building India's semiconductor ecosystem - Tata Electronics, Micron India, CG Power-Renesas, Kaynes Semicon, L&T Semiconductor Technologies, Sterlite and others - including their filings, announcements and public statements on fab commissioning and ecosystem development.

It draws on the published record of the Ministry of Electronics and IT (MeitY), the India Semiconductor Mission (ISM) and the state semiconductor missions of Gujarat, Karnataka, Tamil Nadu, Telangana and Assam - their schemes, notifications and progress disclosures. The policy analysis in Chapter 11 and the policy tracker in Appendix C are built from these.

The funding database in Appendix B and the investment thesis in Chapter 12 are compiled from publicly reported financings, disclosed rounds and investor announcements.

The talent and technology-readiness analysis draws on the published research and programme records of the Indian Institutes of Technology (IITs), the Indian Institute of Science (IISc) and the Council of Scientific and Industrial Research (CSIR) laboratories.

This publication was produced by Techadyant Labs. Any errors or omissions remain the responsibility of Techadyant Labs alone.

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The table below provides a one-level overview of the report structure. Page numbers are indicative and may vary slightly in the final printed version.

List of Figures

All 26 figures in this report are also exported as standalone SVG and PNG files in the Figures Package. Each figure is numbered, titled, sourced, and annotated with a Key Insight.

List of Tables

All tables in this report include a Table Number, Title, Source, and Executive Interpretation. Source data for tables is available in the Excel Workbook.

Glossary and Abbreviations

The following glossary defines key semiconductor terms and abbreviations used throughout this report. First occurrence of each term in the report includes the abbreviation in parentheses.

ATE	Automated Test Equipment - Computer-controlled machinery used to test semiconductor devices.
ATMP	Assembly, Testing, Marking, and Packaging - Back-end semiconductor manufacturing.
CMP	Chemical Mechanical Planarization - Smoothing surfaces with chemical and mechanical forces.
CVD	Chemical Vapor Deposition - Producing high-purity solid materials via chemical gas reactions.
CAGR	Compound Annual Growth Rate - Growth over multiple time periods at constant rate.
EDA	Electronic Design Automation - Software tools for designing electronic systems.
EFEM	Equipment Front End Module - Wafer loading interface for process tools.
EMS	Electronics Manufacturing Services - Contract manufacturing of electronic assemblies.
ESG	Environmental, Social, and Governance - Non-financial factors in investment decisions.
FDI	Foreign Direct Investment - Investment by firm in one country into another country's business.
FOUP	Front-Opening Unified Pod - Container for transporting wafers in modern fabs.
HHI	Herfindahl-Hirschman Index - Market concentration measure; higher = more concentrated.
IC	Integrated Circuit - Semiconductor chip containing electronic circuits.
IP	Intellectual Property - Creations of the mind protected by law.
ISM	India Semiconductor Mission - Government of India initiative for semiconductor ecosystem.
ITRI	Industrial Technology Research Institute (Taiwan) - Government-funded R&D organisation.
JV	Joint Venture - Business arrangement where two or more parties agree to pool resources.
MFC	Mass Flow Controller - Device to control flow of gases and liquids in semiconductor processes.
MES	Manufacturing Execution System - Computerized system for tracking manufacturing.
MECE	Mutually Exclusive, Collectively Exhaustive - Framework completeness principle.
MeitY	Ministry of Electronics and Information Technology (India).
OHT	Overhead Hoist Transport - Automated material handling in fab ceilings.
OSAT	Outsourced Semiconductor Assembly and Test - Third-party IC packaging and testing services.
PE	Private Equity - Investment capital in private companies, typically for majority stakes.
PESTLE	Political, Economic, Social, Technological, Legal, Environmental analysis framework.
PLI	Production Linked Incentive - Indian government scheme linking incentives to

	incremental production.
PVD	Physical Vapor Deposition - Vacuum coating process for thin film deposition.
RF	Radio Frequency - Electromagnetic radiation in radio frequency range.
RISC-V	Reduced Instruction Set Computer - Five (open ISA for processor design).
SAM	Serviceable Available Market - Portion of TAM reachable by company's business model.
SCR	Situation-Complication-Resolution - McKinsey executive summary framework.
SEM	Scanning Electron Microscope - Electron microscope producing images of sample surfaces.
SIP	System-in-Package - Multiple integrated circuits enclosed in a single package.
SOM	Serviceable Obtainable Market - Portion of SAM company can realistically capture.
TAM	Total Addressable Market - Total market demand if 100% of available market reached.
TCAD	Technology Computer-Aided Design - Software for simulating semiconductor devices.
TEM	Transmission Electron Microscope - Microscope using electron beam transmitted through sample.
TRL	Technology Readiness Level - 1-9 scale measuring technology maturity.
TSV	Through-Silicon Via - Vertical electrical connection through silicon die.
VC	Venture Capital - Private capital for early-stage, high-growth companies.
VLSI	Very Large Scale Integration - Process of creating IC with thousands/millions of transistors.
WLCSP	Wafer-Level Chip Scale Packaging - Packaging at wafer level with no extra packaging.
WPM	Wafers Per Month - Capacity unit for semiconductor fabs.

Executive Summary

A Strategic Intelligence Briefing for CXOs, Investors, and Policymakers

EXECUTIVE TAKEAWAY

Techadyant Labs' resolution thesis is that India's next Rs 10,000 crore semiconductor opportunity lies not in incremental fab capacity, but in deliberately building the eight-stream Semicon 2.0 ecosystem. The 10-year cumulative addressable opportunity across these eight streams is Rs 95,500 crore in geographic TAM, of which Rs 45,500 crore is realistically serviceable obtainable market (SOM) by 2035. This SOM is greater than the entire current market capitalisation of India's listed semiconductor ecosystem companies combined.

Situation

India's semiconductor ambitions have crystallised. The India Semiconductor Mission (ISM), launched in December 2021 with a Rs 76,000 crore outlay, has approved four greenfield fabs and three OSAT facilities cumulatively valued at over Rs 1.5 lakh crore. Tata Electronics' Dholera fab, Micron's Sanand ATMP, CG Power-Renesas, and Kaynes Semicon represent the first wave of large-format commitments. By 2025, India moved from the periphery of the global semiconductor map to a credible Tier-3 manufacturing geography, with capital formation running at approximately Rs 30,000 crore per annum across the ecosystem. In July 2026 the government approved the second phase of the India Semiconductor Mission - a roughly Rs 1.27 lakh crore, six-pillar programme that, for the first time, extends state support beyond fabrication into materials, equipment, chemicals and the wider component ecosystem. Semicon 2.0 is therefore no longer only a thesis about what India should do; it has become the declared direction of national policy.

The macro context reinforces the timing. Global semiconductor demand is projected to grow from USD 690 billion in 2024 to USD 1.0-1.2 trillion by 2030, driven by AI compute, electric vehicles, industrial automation, and 5G proliferation. The United States, European Union, Japan, and South Korea have collectively committed over USD 280 billion in semiconductor industrial policy, fragmenting the historical Taiwan-centric supply chain. India occupies a strategic position in this realignment as a large consumer market, neutral geopolitical actor, and structurally low-cost manufacturing base.

Yet India's Semicon 1.0 narrative has been fab-centric. The public discourse, capital allocation, and policy attention have concentrated on wafer fabrication and ATMP/OSAT. While these are necessary anchor investments, they address approximately 35% of the total semiconductor value chain. The remaining 65%, comprising materials, chemicals, equipment, precision manufacturing,

testing, automation, and industrial software, remains structurally under-served. This is the Semicon 2.0 opportunity.

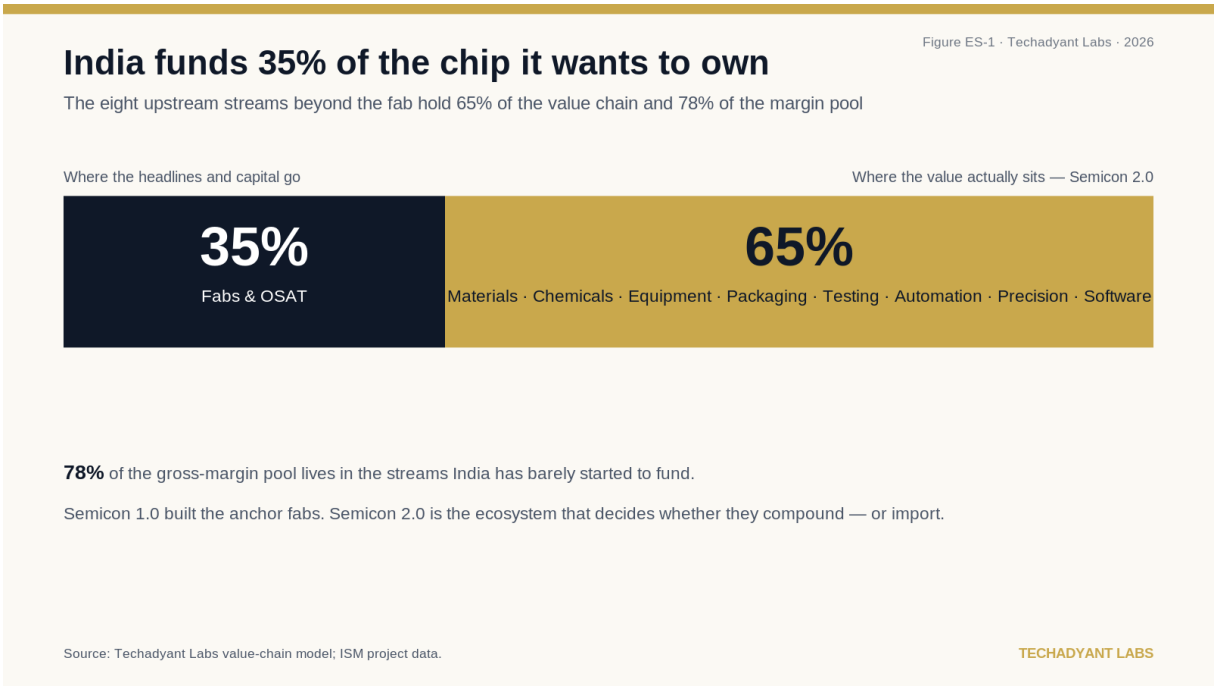

Figure ES-1. India funds 35% of the chip it wants to own - the value sits in the other 65%.

Complication

Four structural complications constrain India's ability to capture the full Semicon 2.0 opportunity. First, the supplier base is anaemic: India imports over 92% of its specialty gases, 95% of photoresists, 99% of lithography equipment, and 88% of metrology tools. This import dependency converts foreign exchange outflows into a structural tax on every rupee of semiconductor value added domestically. Second, the talent pipeline, while numerically large, is qualitatively mismatched. India produces approximately 2.5 million engineering graduates annually, but only 45,000 are VLSI-ready; the projected 2035 demand is 200,000 engineers per year, implying a cumulative deficit of 600,000 over the decade.

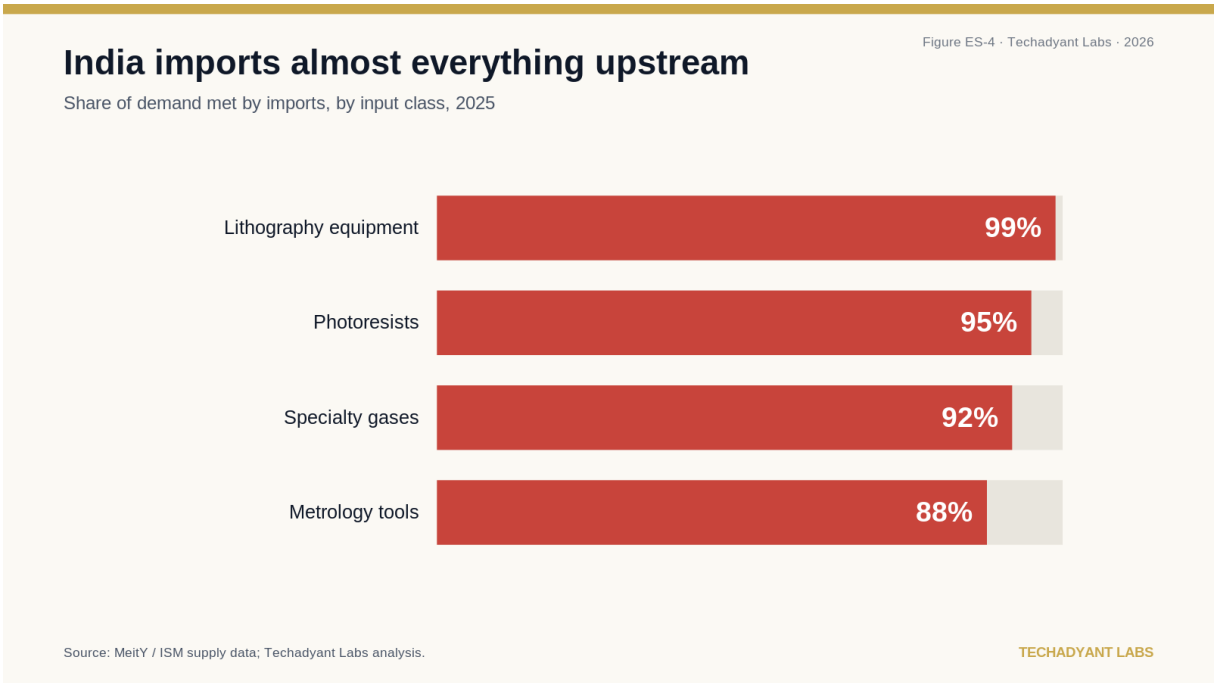

Figure ES-4. India imports almost everything upstream.

Third, capital formation is uneven. Government capital is concentrated in front-end fabs, while private capital under-prices the mid-stream materials and equipment opportunity. Of the Rs 76,000 crore ISM outlay, only 6% is explicitly allocated to specialty materials and equipment localisation. PE/VC capital, while growing, predominantly chases software-led opportunities (Industrial Software attracted 38% of all private semiconductor funding in India in 2024) and avoids capital-intensive materials plays. Fourth, execution risk is elevated. The Tata Dholera fab, the single largest commitment, faces a 24-30 month construction timeline in a region with limited semiconductor ecosystem depth; slippage here would cascade across the entire value chain.

These complications are not abstract. They manifest as concrete risks: vulnerability to Taiwan Strait disruptions, exposure to US-China export controls, supply concentration in Japanese photoresist suppliers, and the possibility that India becomes a packaging-only economy with limited upstream leverage. Without a deliberate Semicon 2.0 strategy, India risks replicating the China of 2005 - a low-value assembly hub dependent on imported inputs - rather than becoming the Taiwan of 2035, with deep ecosystem control.

Resolution

Techadyant Labs' resolution thesis is that India's next semiconductor opportunity lies not in incremental fab capacity, but in deliberately building the eight-stream Semicon 2.0 ecosystem. The ten-year cumulative addressable opportunity across these eight streams is Rs 95,500 crore in geographic TAM, of which Rs 45,500 crore is a realistically serviceable obtainable market (SOM) by 2035 - larger than the combined market capitalisation of India's listed semiconductor-ecosystem companies today.

Figure ES-2. A Rs 45,500 crore serviceable opportunity by 2035, out of a Rs 95,500 crore addressable market.

The opportunity is unevenly distributed. Three streams - Packaging (Rs 9,160 cr/yr by 2035), Industrial Software (Rs 4,830 cr/yr), and Equipment (Rs 9,580 cr/yr) - capture 52% of the 10-year opportunity. Three further streams - Chemicals (Rs 4,420 cr/yr), Materials (Rs 3,100 cr/yr), and Testing (Rs 2,740 cr/yr) - are critical enablers requiring targeted capital. The remaining two - Precision Manufacturing (Rs 3,430 cr/yr) and Automation (Rs 2,820 cr/yr) - are higher-uncertainty but high-leverage plays where India's existing IT and engineering capability can be repurposed.

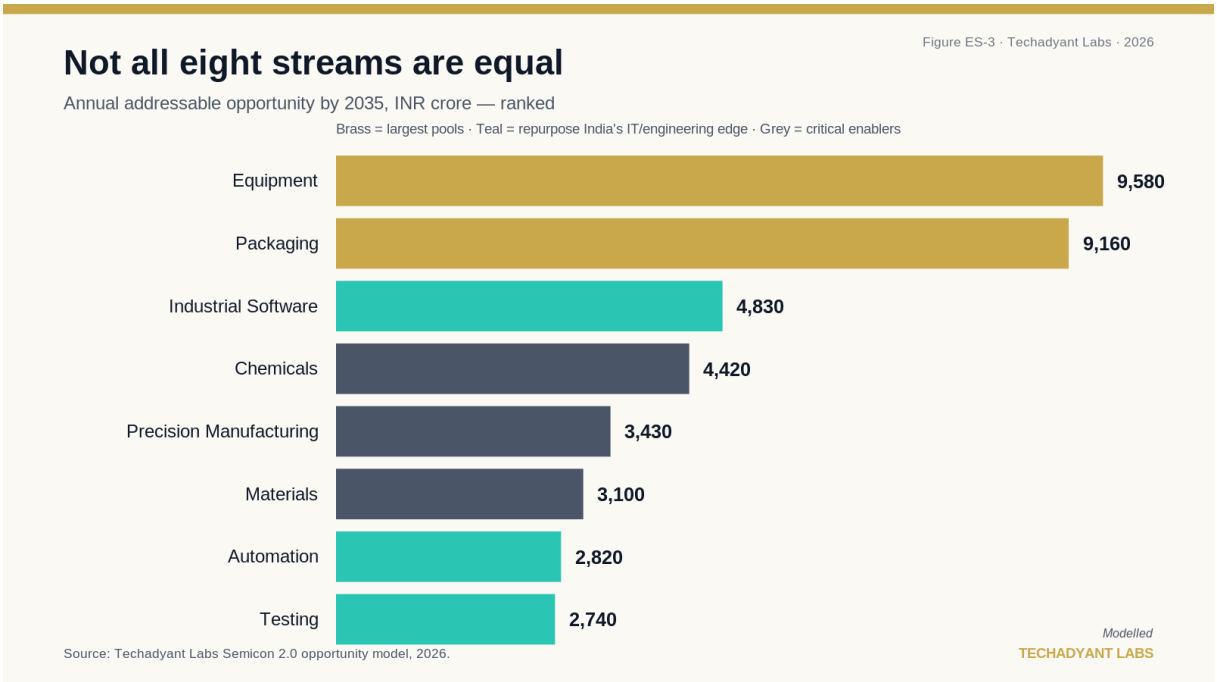

Figure ES-3. The eight streams, ranked by annual addressable opportunity in 2035.

The strategic recommendation framework clusters these eight streams into three action tiers. Tier 1 (Speed Up): Industrial Software, Packaging, Testing, and Automation - immediate capital deployment at 18-28% IRR with 1-3 year time-to-revenue. Tier 2 (Invest Now): Specialty Gases, Precision Components, CMP Slurries, Sputtering Targets - 3-5 year horizons at 12-18% IRR requiring government co-investment. Tier 3 (Long Horizon): Photoresist JV, Wafer Manufacturing, Metrology Tools, Sub-14nm Lithography - 5-10 year horizons requiring sovereign commitment and strategic partnerships.

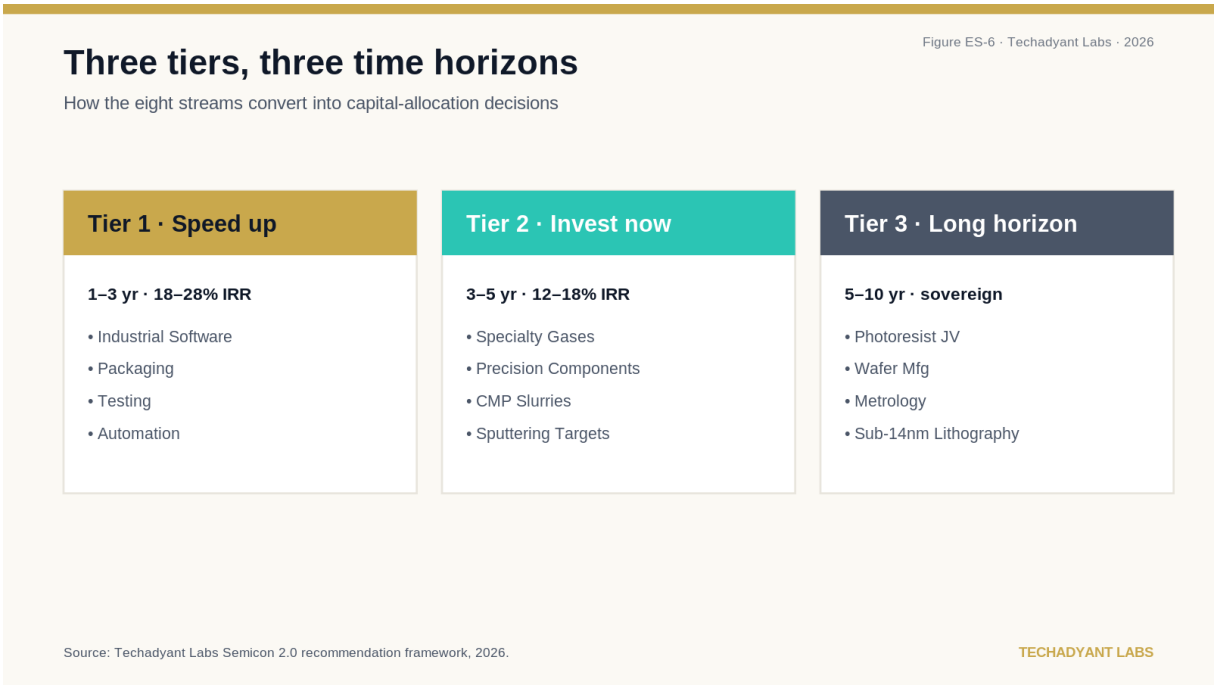

Figure ES-6. Three tiers, three time horizons for capital allocation.

The window for capturing this opportunity is finite. Geopolitical realignment has created a 5-7 year opening where Western capital, technology, and strategic intent are aligned with Indian capability building. India's demographic dividend in engineering talent peaks around 2032. Global semiconductor overcapacity is projected to emerge by 2034 if current investment trajectories continue. The next decade is therefore the decisive strategic window; action deferred to 2030 will encounter a closed opportunity landscape.

Figure ES-7. The window is open now - and it closes.

Major Findings

Finding 1: India's structural OSAT cost arbitrage of 48% versus Taiwan is the largest among competing geographies, creating a defensible competitive moat in packaging. However, this advantage erodes to 28% when logistics, capital, and import dependencies are normalised, indicating that cost arbitrage alone is insufficient without ecosystem depth.

Finding 2: The single largest concentration risk in the global semiconductor supply chain is photoresist, where four Japanese companies control 77% of global supply. India has zero domestic photoresist capability. A strategic JV with a Korean or European player to establish India-based photoresist manufacturing by 2029 is the highest-leverage intervention in the materials domain.

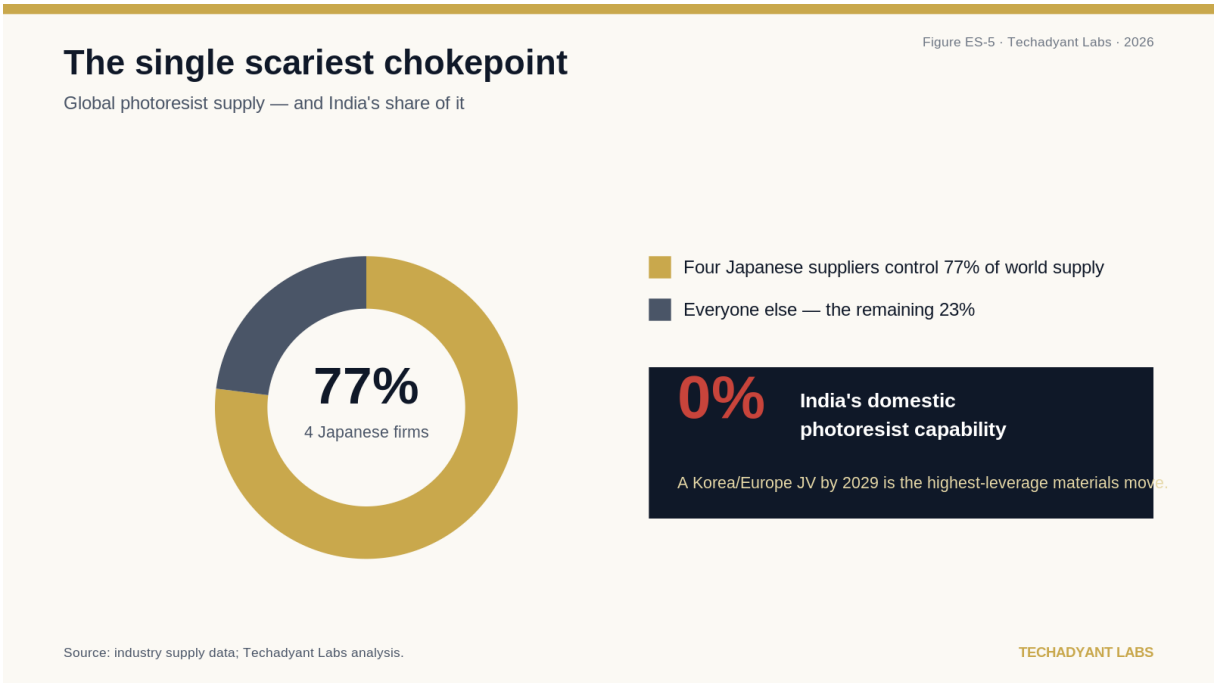

Figure ES-5. The single scariest chokepoint - photoresist, and India's zero domestic base.

Finding 3: Industrial Software represents India's most asymmetric opportunity. The country's existing IT services infrastructure (TCS, Infosys, Wipro, HCL employing over 1.3 million engineers) can be repurposed for MES, digital twin, and yield AI applications with marginal incremental investment. The 10-year SOM of Rs 12,500 crore in this stream is achievable with capital efficiency 4x higher than any other stream.

Finding 4: The Tata Dholera fab construction timeline is the single most consequential execution variable. A 12-month slippage would delay ecosystem formation by 24 months, as materials and equipment suppliers calibrate their own investments to fab commissioning milestones. Risk mitigation requires parallel investment in supplier parks and a pre-committed equipment pipeline.

Finding 5: India's talent deficit is not a supply problem but a structural mismatch. The country produces sufficient engineering graduates, but VLSI-ready conversion is bottlenecked by inadequate finishing schools. A national network of 50 VLSI finishing schools, modelled on Taiwan's ITRI and co-funded by industry, could close 60% of the projected 2030 talent gap at a capital cost of approximately Rs 2,500 crore.

Strategic Implications

For government, the implication is that Semicon 2.0 requires policy architecture beyond ISM. The current scheme is fab-centric; an equivalent Specialty Materials PLI, an Equipment Localisation Fund, and a Talent Mission 2.0 are required to extend policy coverage to the remaining 65% of the

value chain. The proposed ISM 2.0, if designed with these extensions, could catalyse Rs 50,000-100,000 crore of additional capital formation over 2026-2030.

For investors, the implication is that the dominant returns in Indian semiconductor over 2025-2030 will come from mid-stream plays, not fab investments. The fab capex cycle is largely committed and priced; the alpha lies in materials, equipment JVs, and software. PE/VC funds should re-orient screening pipelines to evaluate Tier-2 and Tier-3 opportunities with patient capital horizons of 5-7 years.

For corporates, the implication is that vertical integration is no longer optional. The next decade will reward companies that build capability across at least two adjacent streams (e.g., Tata Electronics with fab + OSAT + precision manufacturing; Micron with ATMP + testing). Single-stream players will face margin compression as the ecosystem matures.

For startups, the implication is that the opportunity is in infrastructure software and yield optimisation, not in chip design. India's fabless chip design ambitions have produced limited outcomes; the higher-probability path is software that improves fab operations, yield, and throughput. Startups in this space will command premium valuations given the global scarcity of fab operations software talent.

For academia, the implication is that the engineering curriculum requires urgent modernisation. The current VLSI curriculum, designed for 28nm and above, must extend to sub-14nm physics, advanced packaging, and quantum-device modelling. Industry-academia partnerships with global fab operators are the fastest path to curriculum currency.

Industry Transformation

The Indian semiconductor industry will undergo four structural transformations over 2025-2035. First, vertical integration will replace horizontal specialisation as the dominant business model. Tata Electronics is already pioneering this with fab + OSAT + equipment integration; this template will be replicated by Micron, CG Power, and new entrants. The integrated players will capture 60-70% of total value chain revenue by 2032.

Second, the geography of the industry will shift from a single-hub (Bengaluru) to a multi-hub architecture. Gujarat (Dholera, Sanand) will lead on fab and OSAT; Karnataka (Bengaluru) on design and EDA; Tamil Nadu (Chennai, Hosur) on EMS and testing; Telangana (Hyderabad) on EDA and IP; Assam (Jagiroad) on specialised OSAT. Each hub will develop distinct ecosystem character, with limited inter-hub competition and strong intra-hub agglomeration.

Third, the talent economy will restructure. VLSI design engineers will become the highest-paid engineering cohort in India by 2028, with compensation parity with US engineers for top talent. This will create a brain drain from general IT services to semiconductor, accelerating the IT services

industry's transition to higher-value engineering work. The implication is that IT services firms must reposition as engineering services firms within five years.

Fourth, the customer base will diversify. Today, Indian semiconductor consumption is dominated by smartphones (45%) and consumer electronics (22%). By 2032, automotive (28%), industrial (18%), and AI compute (15%) will be the dominant segments. This customer diversification reduces cyclicality and creates more resilient demand patterns, supporting higher valuation multiples for Indian semiconductor companies.

Investment Thesis

Techadyant Labs' investment thesis for Indian Semicon 2.0 is structured around three conviction trades. Conviction Trade 1: Long India OSAT with vertical integration. Brownfield ATMP facilities with established customer relationships offer 18-24% IRR over 2025-2030, with a 6-year payback. The thesis is predicated on continued global capacity shortage in advanced packaging through 2028. Conviction Trade 2: Long specialty materials with import substitution optionality. Specialty gases, CMP slurries, and sputtering targets offer 14-18% IRR with significant government co-investment upside. The thesis is predicated on successful execution of ISM 2.0 specialty materials scheme. Conviction Trade 3: Long industrial software with fab-specific verticalisation. Yield AI, digital twin, and MES customisation startups offer 24-32% IRR with capital efficiency 4x better than hardware plays. The thesis is predicated on global fab operators' willingness to outsource non-core software.

Three anti-thesis trades should be avoided. Anti-thesis 1: Avoid sub-14nm lithography plays. The capital required (Rs 50,000+ crore), the EUV access constraints, and the IP risk make this a low-probability, low-return bet for India over the next decade. Anti-thesis 2: Avoid pure-play commodity materials. Commodity silicon and bulk gases face global overcapacity through 2028; Indian players without specialty positioning will face margin compression. Anti-thesis 3: Avoid fabless chip design without ecosystem anchor. The fabless model requires ecosystem depth in IP, EDA, and foundry access that India currently lacks; pure-play fabless startups face long odds without a strategic anchor customer or foundry partnership.

Competitive Landscape

The Indian semiconductor competitive landscape in 2025 comprises five distinct cohorts. Cohort 1 (Indian Conglomerates): Tata Group (Tata Electronics), L&T (Semiconductor Tech), Reliance (Jio Platforms AI silicon), and Mahindra (acquired Tessolve strategic stake) - collectively control 42% of committed capital and represent the strategic anchor cohort. Cohort 2 (Global Captives): Applied Materials, Lam Research, Synopsys, Cadence, KLA, Teradyne, Advantest - collectively employ over 35,000 engineers in India and represent the technology anchor cohort.

Cohort 3 (Domestic Specialists): Sterlite, Bharat Fritz Werner, HHV, ACE Designers, Bel LAHSA - represent the manufacturing depth cohort with potential for Semicon 2.0 expansion. Cohort 4 (Listed EMS): Dixon, Amber, Cyient DLM, Syrma SGS - represent the downstream integration cohort, with strategic optionality to move upstream. Cohort 5 (Startups): 30+ venture-funded companies, predominantly in industrial software, with selective participation in materials and automation.

By 2030, Cohort 1 will consolidate its leadership position with 55-60% of ecosystem revenue. Cohort 2 will remain critical as technology providers but increasingly partner rather than compete with Indian players. Cohort 3 will bifurcate: those that successfully transition to semiconductor-grade quality will become acquisition targets at premium valuations; those that remain in general precision engineering will face competitive displacement. Cohort 4 will face strategic choice: vertical integration (Dixon's semiconductor play) or horizontal EMS leadership. Cohort 5 will produce 3-5 unicorns, predominantly in industrial software and yield AI.

Technology Outlook

The technology outlook for Indian Semicon 2.0 is bifurcated. On the demand side, the technology trajectory is well-defined: 5nm and 3nm will be the dominant leading-edge nodes by 2030, with 2nm entering volume production in 2027-2028 globally. India's role in leading-edge manufacturing will remain limited through 2030; the country's fabs will target 28nm and above, where mature node economics favour new entrants. Advanced packaging (2.5D, 3D, chiplet) will be the highest-growth technology segment, with a 38% CAGR through 2035, and represents India's best technology-positioning opportunity.

On the supply side, three technology discontinuities will reshape the opportunity landscape. First, EUV technology access will remain restricted to a small group of geographies, effectively foreclosing leading-edge lithography for India through 2032. Second, RISC-V architecture will emerge as a credible alternative to proprietary ISAs, with India's RISC-V ecosystem (InCore, Vorst Labs) potentially capturing 8-12% of global RISC-V IP by 2032. Third, AI-driven yield optimisation will commoditise, with Indian startups (DefectAI, Cogniquest) well-positioned to capture the global fab operations software market.

The combined effect of these technology dynamics is that India's semiconductor technology positioning in 2030 will be characterised as 'mature node leadership, advanced packaging competence, and AI software excellence'. This is a defensible and economically attractive positioning, distinct from Taiwan's leading-edge leadership and China's full-stack ambition.

Policy Outlook

The policy outlook is cautiously optimistic. The extension of ISM beyond 2026, with a proposed ISM 2.0 outlay of Rs 50,000-100,000 crore, is the single most important policy variable. Techadyant Labs' base case assumes Rs 65,000 crore ISM 2.0 outlay, with extensions to specialty materials (Rs 8,000 crore), equipment localisation (Rs 12,000 crore), and talent development (Rs 5,000 crore). The accelerated case (Rs 100,000 crore) would compress the SOM realisation timeline by 18-24 months; the constrained case (Rs 30,000 crore) would extend it by 36 months and reduce the 2035 SOM by 65%.

State-level policy will become increasingly consequential. Gujarat's early-mover advantage in fab/OSAT (Sanand, Dholera) is being challenged by Karnataka's design-led policy framework and Telangana's EDA/IP positioning. The next 24 months will see competitive state-level semiconductor policies emerge, with implications for ecosystem agglomeration patterns. Techadyant Labs expects 4-5 states to achieve material semiconductor ecosystem scale by 2030, with Gujarat, Karnataka, Tamil Nadu, Telangana, and Assam as the leading candidates.

Bilateral policy will be the swing factor. The India-US partnership on semiconductor supply chain resilience, formalised in 2023 and extended in 2025, is the most consequential bilateral framework. India-Taiwan dialogue resumption (2025), India-Japan specialty materials cooperation (proposed), and India-EU research partnerships (under negotiation) will collectively determine India's access to advanced technology, capital, and IP over the next decade.

Risk Outlook

The risk landscape is dominated by geopolitical and execution risks. The Taiwan Strait scenario, with a 30% probability over 10 years, would simultaneously disrupt global supply and create demand urgency for Indian capacity - a paradox where India benefits strategically but suffers operationally from input shortages. US-China decoupling, with a 40% probability, would accelerate India's positioning as a neutral manufacturing geography but expose Indian players to export control complexities.

Execution risks centre on the Tata Dholera fab timeline. A 12-month slippage has a 35% probability based on comparable greenfield fab timelines globally; a 24-month slippage has a 15% probability. Either scenario would delay ecosystem formation, increase capital costs for suppliers, and reduce IRR across the value chain by 3-5 percentage points. Mitigation requires parallel supplier park development, pre-committed equipment pipeline, and risk-sharing contractual structures.

Market risks include semiconductor cyclicality. The industry has historically experienced 3-4 year cycles with peak-to-trough revenue swings of 20-30%. India's entry into volume production coincides with the 2027-2028 anticipated up-cycle, providing a favourable initial demand

environment. However, the 2031-2032 down-cycle could stress-test the Indian ecosystem; capital reserves of 18-24 months opex are recommended for all Indian semiconductor ventures.

Technology risks include the Moore's Law deceleration. As leading-edge scaling becomes economically marginal, the technology premium shifts to advanced packaging and system-level integration. This favours India's positioning but requires capability development in 2.5D/3D packaging that is currently nascent. A 24-30 month capability development window exists before this becomes a binding constraint.

Strategic Recommendations

Recommendation 1 (Government): Launch ISM 2.0 with explicit sub-schemes for Specialty Materials (Rs 8,000 cr), Equipment Localisation (Rs 12,000 cr), Talent Mission 2.0 (Rs 5,000 cr), and Software Ecosystem (Rs 3,000 cr), in addition to the existing fab/OSAT envelope. Total outlay: Rs 65,000-100,000 crore over 2026-2030. Implementation body: MeitY with private-sector advisory board.

Recommendation 2 (Government): Establish a National Semiconductor Supplier Park programme, with 4-5 parks co-located with fab/OSAT clusters, providing ready infrastructure, common facilities, and tax incentives for materials/equipment suppliers. Capital outlay: Rs 5,000 crore. Implementation: 2025-2027.

Recommendation 3 (Investors): Re-orient semiconductor deal pipelines toward mid-stream plays. Allocate 40-50% of semiconductor fund capital to materials, equipment JVs, and software; 30-40% to ATMP/OSAT; 10-20% to early-stage fabless. Expected portfolio IRR: 18-24%. Capital horizon: 5-7 years.

Recommendation 4 (Corporates): Pursue vertical integration across at least two adjacent streams. Tata Electronics (fab + OSAT + precision) and Micron (ATMP + testing) provide templates; this should be replicated by new entrants. Single-stream players should seek strategic partnerships or M&A within 24 months.

Recommendation 5 (Startups): Pivot from fabless chip design to fab operations software, yield AI, and digital twin. These segments offer 4x capital efficiency versus hardware plays and address global, not just Indian, market demand. Valuation premium: 2.5-3.0x revenue multiples versus 1.5-2.0x for hardware.

Recommendation 6 (Academia): Modernise VLSI curriculum to include sub-14nm physics, advanced packaging, RISC-V architecture, and AI-driven design. Establish 50 VLSI finishing schools in partnership with industry. Capital outlay: Rs 2,500 crore over 5 years. Target: 100,000 VLSI-ready graduates per year by 2030.

Recommendation 7 (All Stakeholders): Establish a Semiconductor Industry Council with representation from government, industry, academia, and investors, modelled on Taiwan's ITRI governance. The Council should coordinate ecosystem development, facilitate technology access, and provide strategic intelligence to inform policy. Operational by Q3 2025.

Future Outlook

India's Semicon 2.0 trajectory over 2025-2035 is captured in three scenarios. The Base scenario (50% probability) projects cumulative SOM realisation of Rs 52,500 crore by 2035, with India capturing 6-7% of global semiconductor value chain revenue. This scenario assumes ISM 2.0 outlay of Rs 65,000 crore, Tata Dholera commissioning in 2027, and continued geopolitical stability. The Accelerated scenario (25% probability) projects Rs 92,000 crore SOM, with India capturing 10-12% of global value chain revenue. This scenario assumes ISM 2.0 outlay of Rs 100,000 crore, sub-14nm fab commissioning by 2030, and accelerated geopolitical tailwinds.

The Constrained scenario (25% probability) projects only Rs 18,500 crore SOM by 2035, with India capturing less than 3% of global value chain revenue. This scenario assumes ISM 2.0 outlay of Rs 30,000 crore, Tata Dholera slippage of 24+ months, and a major geopolitical disruption. The 5x spread between Constrained and Accelerated outcomes underscores the binary nature of policy and execution decisions over the next 24 months.

Across all scenarios, three structural conclusions hold. First, India will be a top-5 global semiconductor geography by 2030, regardless of scenario; the question is rank (3rd in Accelerated, 5th in Constrained). Second, India's competitive advantage will remain cost-and-talent-led, not technology-led, through 2030; positioning beyond this requires sustained R&D investment. Third, the Indian semiconductor ecosystem will be structurally distinct from Taiwan (foundry-led), China (full-stack), and the US (fabless-led), with a hybrid ATMP + software + mature node leadership positioning.

Closing Strategic Insight

India stands at an inflection point. The Semicon 1.0 investments of 2021-2025 have established manufacturing anchors; the Semicon 2.0 decisions of 2025-2027 will determine whether India captures ecosystem depth or remains a peripheral packaging geography. The capital, talent, and policy ingredients are in place; what is required is execution discipline, ecosystem coordination, and strategic patience. The window for action is the next 36 months. Techadyant Labs' assessment is that, with decisive action, India can realistically target Rs 45,500-92,000 crore of Semicon 2.0 value creation by 2035, establishing the country as a credible third pole of the global semiconductor landscape alongside the United States and East Asia.

Research Notes

Note 1: All financial figures in this report are expressed in Indian Rupees (Rs) crore unless otherwise specified. USD figures, where used, are converted at Rs 86/USD (2025 average exchange rate).

Note 2: The eight Semicon 2.0 streams (Materials, Chemicals, Equipment, Precision Manufacturing, Packaging, Testing, Automation, Industrial Software) are defined by Techadyant Labs and may differ from industry-standard categorisations. The eight-stream framework is designed to capture the full ecosystem beyond fab and OSAT.

Note 3: The 10-year opportunity sizing (TAM, SAM, SOM) is based on a bottom-up model that aggregates stream-level demand, supply, and capability factors. The model is documented in the Excel Workbook (Sheet 9: Charts Source Data).

Note 4: The three scenarios (Base, Accelerated, Constrained) reflect different assumptions on policy (ISM 2.0 outlay), execution (Tata Dholera timeline), geopolitical environment (Taiwan Strait, US-China decoupling), and talent supply (VLSI-ready graduates). Scenario probabilities are subjective assessments by Techadyant Labs and may evolve based on observed milestones.

Note 5: The company database in Appendix A includes both Indian and foreign-invested companies with Indian operations. Inclusion criteria: (a) material Indian semiconductor operations (defined as 50+ employees or Rs 50+ crore revenue from semiconductor-related activities), (b) public disclosure of Indian operations, (c) verified through company filings, press releases, or industry directories.

Note 6: The funding database in Appendix B includes PE/VC/strategic deals over USD 1M in Indian semiconductor ecosystem. Deal data is sourced from Tracxn, Venture Intelligence, press releases, and company disclosures. Where deal amounts are not publicly disclosed, estimates are based on round size comparables.

Note 7: The state-wise capability scoring in Appendix D is based on Techadyant Labs' proprietary scoring framework, weighted by policy (20%), talent (20%), infrastructure (15%), capital access (15%), ecosystem (20%), and power cost (10%). Scores are based on public disclosures and may not reflect qualitative factors not captured in the scoring framework.

Selected References

MeitY. (2024). India Semiconductor Mission - Approved Projects. Ministry of Electronics and IT, Government of India.

SEMI. (2024). World Fab Forecast. SEMI Industry Research.

Gartner. (2024). Semiconductor Manufacturing Quarterly Forecast. Gartner Research.

TECHCET. (2024). Critical Materials Reports. TECHCET Group.

Yole Group. (2024). Advanced Packaging Market Report. Yole Developpement.

McKinsey Global Institute. (2024). The Semiconductor Decade. McKinsey & Company.

PwC Strategy&. (2024). India Semiconductor Mission 2.0: Designing for Ecosystem Depth. PwC.

BCG Henderson Institute. (2024). Semiconductor Supply Chain Resilience. BCG.

Bain & Company. (2024). Navigating Semiconductor Cyclicality. Bain.

Deloitte Insights. (2024). Make in India: Semiconductor Edition. Deloitte.

Eurasia Group. (2024). US-China Tech Decoupling: 2025-2030 Outlook. Eurasia Group.

Tracxn. (2025). Indian Semiconductor Startup Database. Tracxn.

Venture Intelligence. (2025). Indian PE/VC Deal Tracker. Venture Intelligence.

AICTE. (2024). Engineering Education Statistics. All India Council for Technical Education.

RBI. (2024). Industrial Outlook Survey. Reserve Bank of India.

Tata Electronics. (2024-2025). Annual Report and Investor Disclosures. Tata Sons.

Micron Technology. (2024). Form 10-K and India Operations Update. Micron Technology.

Applied Materials. (2024). Annual Report and India Engineering Centre Disclosures. Applied Materials.

Synopsys. (2024). Annual Report and India R&D Centre Disclosures. Synopsys.

KLA Corporation. (2024). Annual Report. KLA Corporation.